MODELLING OF TOWERING SPEED AND AREA COMPETENT VEDIC MULTIPLIER

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ABSTRACT

High speed pipelined multiplier architecture is proposed in this paper. The pipelined architecture consists of 3 stages. 1st stage consists of the 4 - bit Vedic Multiplication unit. 2nd stage consists of partial products and carry. 3rd stage consists of adders and the result of the multiplication. This paper presents the efficiency of Urdhva Tiryakbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates complex multiplication steps. The proposed algorithm is modeled using VHDL, a hardware description language. It is found that 11 logic cells are required to build nibble multiplier. The propagation time of the proposed architecture is found to be 4.585ns. Implementation has been done for the Xilinx FPGA device, Spartan-3E. The layout is designed by using Microwind. The results shows that multiplier implemented using Vedic multiplication is efficient in terms of area and speed compared to its implementation using Array and Booth multiplier architectures.

KEYWORDS: Vedic Mathematics, Urdhva Triyakbhyam Sutra, Array Multiplier, Booth Multiplier, Nibble, High Speed